Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A processor for use in a Voice-over-Internet Protocol telephone, including:

a Voice-over-Internet Protocol processor core operable to transmit computer data and voice data over a computer network, the processor core including one or more pipelines;

a bus on which signals internal to the processor are routed;

an on-chip memory coupled to the Voice-over-Internet Protocol processor core through the bus, the on-chip memory including a program memory to include instruction and a data memory to store cache for the processor core;

one or more communication ports coupled to the Voice-over-Internet Protocol processor core and memory through the bus;

a repeater coupled to the Voice-over-Internet Protocol processor core through the bus; and

one or more IEEE 802.3 media access controllers (MACs) coupled to the Voice-over-Internet Protocol processor core through the bus, the one or more MACs being separate from the Voice-over-Internet Protocol processor core,

wherein the Voice-over-Internet Protocol processor core transmits the computer data and the voice data through the one or more communication ports, and wherein the repeater, the one or more communication ports and the one or more IEEE 802.3 MACs are each integrated onto a same chip as the Voice-over-Internet Protocol processor core.

2. (Previously Presented) The processor of claim 1, wherein the one or more communication ports further include one or more pulse code modulation (PCM) ports.

3. (Cancelled)

4. (Previously Presented) The processor of claim 1, wherein the one or more communication ports further include one or more universal serial bus (USB) ports.

5. (Previously Presented) The processor of claim 1, wherein the one or more communication ports allow the Voice-over-Internet Protocol processor core to be coupled to one or more external components without external interfacing circuitry.

6. (Currently amended) An apparatus, comprising:

a single-chip Voice-over-Internet Protocol network processor operable to transmit computer data and voice data over a computer network, the single-chip Voice-over-Internet Protocol network processor including,

a flexible peripheral interconnect (FPI) bus;

one or more universal serial bus (USB) ports integrated onto the single chip through the FPI bus, the one or more USB ports operable to provide an interface between the Voice-over-Internet Protocol network processor and one or more USB compatible devices without having to provide external interfacing circuitry;

a repeater integrated onto the single chip through the FPI bus; and

one or more IEEE media access controllers (MACs) integrated onto the single chip through the FPI bus, the one or more MACs being separate from the single chip Voice-over-Internet Protocol network processor.

7. (Cancelled)

8. (Previously Presented) The apparatus of claim 6, wherein the single-chip Voice-over-Internet Protocol network processor further includes one or more pulse code modulation (PCM) ports integrated onto the single chip through the FPI bus.

9. (Previously Presented) The apparatus of claim 8, wherein each PCM port is operable to handle up to 30 time slots, and wherein each time slot is capable of handling a 64K bit/sec voice channel.

10. (Currently amended) A system, comprising:

a single-chip Voice-over-Internet Protocol network processor operable to transmit computer data and voice data over a computer network, the single-chip Voice-over-Internet Protocol network processor including,

a flexible peripheral interconnect (FPI) bus;

one or more universal serial bus (USB) ports integrated onto the single chip through the FPI bus, the one or more USB ports operable to provide an interface between the Voice-over-Internet Protocol network processor and one or more USB compatible devices without having to provide external interfacing circuitry;

a repeater integrated onto the single chip through the FPI bus;

one or more IEEE media access controllers (MACs) integrated onto the single chip through the FPI bus, the one or more MACs being separate from the single chip Voice-over-Internet Protocol network processor; and

a memory unit coupled to the Voice-over-Internet Protocol network processor, the memory unit operable to store programs used by the Voice-over-Internet Protocol network processor.

11. (Cancelled)

12. (Previously Presented) The system of claim 10, wherein the single-chip Voice-over-Internet Protocol network processor further includes one or more pulse code modulation (PCM) ports integrated onto the single chip through the FPI bus.

13. (Previously Presented) The system of claim 12, wherein each PCM port is operable to handle up to 30 time slots, and wherein each time slot is capable of handling a 64K bit/sec voice channel.

14. (Previously Presented) The system of claim 12, further comprising a digital-to-analog/analog-to-digital (DA/AD) converter connected to the single-chip Voice-over-Internet Protocol network processor through one of the one or more pulse code modulation (PCM) ports integrated onto the single chip.

15. (Previously Presented) The system of claim 14, further comprising a microphone, a speaker, and a handset, each connected to the single-chip Voice-over-Internet Protocol network processor through the DA/AD converter.

16. (Previously Presented) The system of claim 15, further comprising a keypad interfaced with the single-chip Voice-over-Internet Protocol network processor, the keypad operable to allow a user to dial telephone numbers.

17. (Previously Presented) The system of claim 16, further comprising a liquid crystal display (LCD) operable to display information entered through the keypad.

18. (Cancelled)

19. (Previously Presented) The processor of claim 1, wherein at least one pipeline supports one of arithmetic, load and store, and loop control operations for the processor core.

20. (Previously Presented) The processor of claim 1, wherein at least one pipeline is configured to execute at least one of integer instructions, bit operations, MAC instructions and conditional data jumps.

21. (Previously Presented) The processor of claim 1, wherein at least one pipeline is configured to executes load and store instructions, context operations, system instructions, address arithmetic and conditional and unconditional address instructions for the processor core.

22. (Previously Presented) The processor of claim 1, wherein at least one pipeline includes a loop hardware cache buffer operable to store location, target and minimal set of information required to execute repetitive loop within the at least one pipeline so as to achieve loop optimization.

23. (Previously Presented) The processor of claim 1, wherein the processor core includes separate address and data buses for the program memory and the data memory.

24. (Previously Presented) The system of claim 10, wherein the FPI bus is a demultiplexed, pipelined bus.